the second step of forming a gate oxide film and a gate electrode on said semiconductor substrate in said element active region;

the third step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming an insulating interlayer on an entire surface of said semiconductor substrate;

the fifth step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed;

the sixth step of forming a first conductive film on said insulating interlayer which fills said hole electrically connected to one of said impurity diffusion layers covering;

the seventh step of forming a mask pattern having at least first and second openings on said first conductive film;

the eighth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a hole extending through said first conductive film below said second opening, said first conductive film is etched until said insulating interlayer is exposed in said first opening;

the ninth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the tenth step of forming a second conductive film so as to cover said dielectric film opposing said first conductive film through said dielectric film.

44. (Amended) A method according to claim 42, further comprising, between the sixth and seventh steps of planarizing said first conductive film by polishing.